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Amendments to the Specification

Please replace the Abstract with the following rewritten Abstract:

ABSTRACT

Techniques are described for efficient reordering of data and performing data exchanges within a register file or memory, or in general, any device storing data that is accessible through a set of addressable locations. In one technique, an address translator is placed in the path of all or a selected set of address busses to a storage device to provide a programmable ~~and selectable means of~~ translating of the storage device addresses. An effect of this translation is that the data stored in one pattern may be accessed and stored in another pattern or accessed, processed and stored in another pattern. The address translation operation may be carried out in a single cycle, does not involve the physical movement of data in swap operations, allows data to effectively be ordered more efficiently for algorithmic processing and therefore saves power. Address translation functions are shown to be useful for vector operations and a new type of storage unit using built in address translation functions is presented.